



NI Research Framework Systems

Massive MIMO & 5G Application Development



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Overview

Massive multiple input, multiple output (MIMO) is an exciting area of 5G wireless research. For next-generation wireless data networks, it promises significant gains that offer the ability to accommodate more users at higher data rates with better reliability while consuming less power. Using the NI Massive MIMO Application Framework, researchers can build scalable antenna count MIMO testbeds to rapidly prototype large-scale antenna systems using award-winning LabVIEW system design software and state-of-the-art NI USRP™ RIO software defined radios (SDRs).

With a simplified design flow for creating FPGA-based logic and streamlined deployment for high-performance processing, researchers in this field can meet the demands of prototyping these highly complex systems with a unified hardware and software design flow.

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Introduction and need for Massive MIMO

Exponential growth in the number of mobile devices and the amount of wireless data they consume is driving researchers to investigate new technologies and approaches to address the mounting demand. The next generation of wireless data networks, called the fifth generation or 5G (<http://www.ni.com/5g>), must address not only capacity constraints but also existing 5G challenges—such as network reliability, coverage, energy efficiency, and latency—with current communication systems. Massive MIMO, a candidate for 5G technology, promises significant gains in wireless data rates and link reliability by using large numbers of antennas (more than 64) at the base transceiver station (BTS). This approach radically departs from the BTS architecture of current standards, which uses up to eight antennas in a sectorized

topology. With hundreds of antenna elements, massive MIMO reduces the radiated power by focusing the energy to targeted mobile users using precoding techniques. By directing the wireless energy to specific users, radiated power is reduced and, at the same time, interference to other users is decreased. This is particularly attractive in today's interference-limited cellular networks. If the promise of massive MIMO holds true, 5G networks of the future will be faster and accommodate more users with better reliability and increased energy efficiency.

With so many antenna elements, massive MIMO has several system challenges not encountered in today's networks. For example, today's advanced data networks based on LTE or LTE-Advanced require pilot overhead proportional to the number of antennas. Massive MIMO manages overhead for a large number of antennas using time division duplexing (TDD) between uplink and downlink assuming channel reciprocity. Channel reciprocity allows channel state information obtained from uplink pilots to be used in the downlink precoder. Additional challenges in realizing massive MIMO include scaling data buses and interfaces by an order of magnitude or more and distributed synchronization amongst a large number of independent RF transceivers.

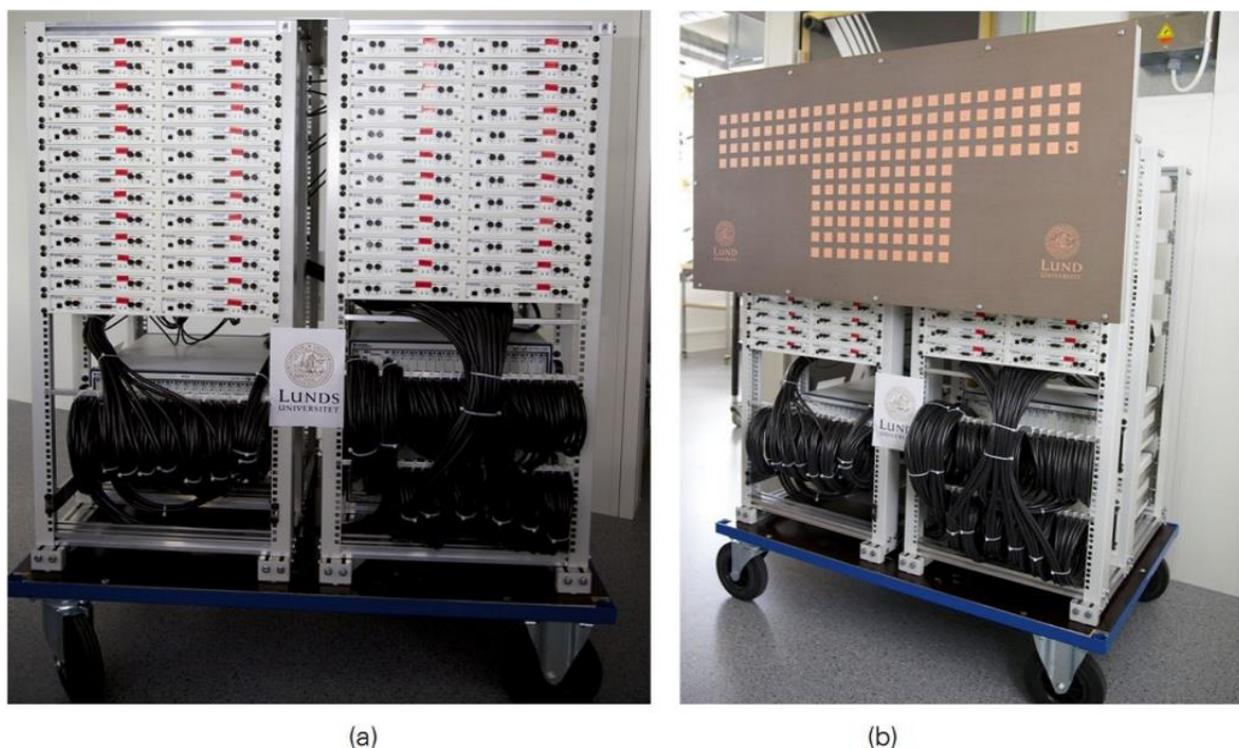


Figure 1- An example massive MIMO testbed at Lund University in Sweden is based on USRP RIO (a) with a custom cross-polarized patch antenna array (b).

These timing, processing, and data collection challenges make prototyping vital. For researchers to validate theory, this means moving from theoretical work to testbeds. Using real-world waveforms in real-world scenarios, researchers can develop prototypes to determine the feasibility and commercial viability of massive MIMO. As with any new wireless standard or technology, the transition from concept to prototype

impacts the time to actual deployment and commercialization. And the faster researchers can build prototypes, the sooner society can benefit from the innovations.

Possible Research Topics with Massive MIMO Systems:

In this section; the intention is to list some research problems that may fall under the subjects of Massive MIMO research. These lists might serve as an accessible entry-point for those who want to study these fields using the proposed framework.

Massive MIMO networks will be structured by the following key elements:

- i. Antennas and antenna arrays
- ii. Electronic components,
- iii. Network architectures,
- iv. Protocols and signal processing.

Each of these elements are open for research and further development. Except the foundational RF electronic components; the proposed framework system could be used during the prototyping and development of above key elements of the massive MIMO systems.

The first important ingredient of massive MIMO networks is antenna technology; which implies designers to assemble large antenna arrays with various requirements in terms of spacing of elements and geometries, reducing the number of required radio frequency (RF) chains at the transmit and the receive ends and their implementation costs. In certain scenarios and deployments, the use of compact antennas with closely-spaced elements will be of great importance to equip devices with a large number of antennas but this will require techniques to mitigate the coupling effects especially at the user terminals. Proposed framework systems include omnidirectional antennas for low-channel count variants but due to coupling effects; different antenna solutions are advised for higher channel count systems.

The second key area for innovation is that of electronic components and RF chains, where the use of lowcost amplifiers with output power in the mWatt range will play an important role. Existing peripherals such as large coaxial cables and power-hungry circuits will have to be replaced with low-energy solutions.

Another key element of massive MIMO networks is the network architecture, which will evolve from homogeneous cellular layouts to heterogeneous architectures that include small cells and the use of coordination between cells. Since massive MIMO technology is likely to be incorporated into cellular and local area networks in the future, the network architecture will necessitate special attention on how to manage the interference created and measurements campaigns will be of fundamental importance. System studies into coexistence with small cells and heterogeneous network solutions are gaining more attention as well.

The last ingredient of massive MIMO networks and the main focus of the proposed framework system is signal processing. In particular, MIMO signal processing will play a crucial role in dealing with the impairments of the physical medium and in providing cost-effective tools for processing information. Current state-of-the-art in MIMO signal processing requires a computational cost for transmit and receive processing that grows as a cubic or super-cubic function of the number of antennas, which is clearly not scalable with a large number of antenna elements using the conventional CPU/GPU based solutions. FPGA based designs are likely to be more and more dominant due to their inherent parallel nature and thanks to the recent developments in silicon-fabric and also system level design tools such as LabVIEW FPGA. FPGAs have long been used in wireless infrastructure equipment to implement complex signal-processing algorithms

and they will be used for prototyping 5G wireless infrastructure over the next few years. There really are no other alternatives.

1. Massive MIMO Prototype Synopsis

Outlined below is a complete Massive MIMO Application Framework. It includes the hardware and software needed to build the world's most versatile, flexible, and scalable massive MIMO testbed capable of real-time, two-way communication over bands and bandwidths of interest to the research community. With NI software defined radios (SDRs) and LabVIEW system design software, the modular nature of the MIMO system allows for growth from only a few nodes to a 128-antenna massive MIMO system. With the flexible hardware, it can be redeployed in other configurations as wireless research needs evolve over time, such as distributed nodes in an ad-hoc network, or as multi-cell coordinated networks.

Using SDR concepts, NI and Lund University research teams developed the system software and physical layer (PHY) using an LTE-like PHY and TDD for mobile access. The software developed through this collaboration is available as the software component of the Massive MIMO Application Framework.

Table 1 shows the system and protocol parameters supported by the Massive MIMO Application Framework. Table 1 shows the system and protocol parameters supported by the Massive MIMO Application Framework.

Parameter	Values
Number of BTS Antennas	Scalable. Sample code exists for configurations between 8 to 128
RF Center Frequency	1.2 GHz. ÷ 6 GHz.
Bandwidth per Channel	20 MHz.
Sampling Rate	30.72 MS/sec
FFT Size	2048
Number of Used Sub-Carriers	1024
Slot Time	0.5 msec
User Sharing Time per Frequency Slot	10

Table 1 - Massive MIMO Application Framework System Parameters

2. Massive MIMO System Architecture

A massive MIMO system, as with any communication network, consists of the BTS and user equipment (UE) or mobile users. Massive MIMO envisioned for cellular applications, consists of the BTS and user equipment (UE) or mobile users.

Massive MIMO, however, departs from the conventional topology by allocating a large number of BTS antennas to communicate with multiple UEs simultaneously. In the system that NI and Lund University developed, the BTS uses a system design factor of 10 base station antenna elements per UE, providing 10 users with simultaneous, full bandwidth access to the 100 antenna base station. This design factor of 10 base station antennas per UE has been shown to allow for most theoretical gains to be harvested.

In a massive MIMO system, a set of UEs concurrently transmit an orthogonal pilot set to the TS. The BTS received uplink pilots can then be used to estimate the channel matrix. In the downlink time slot, this channel estimate is used to compute a precoder for the downlink signals. Ideally, this results in each mobile user receiving an interference-free channel with the message intended for them. Precoder design is an open area of research and can be tailored to various system design objectives. For instance, precoders can be designed to null interference at other users, minimize total radiated power, or reduce the peak to average power ratio of transmitted RF signals.

Although many configurations are possible with this architecture, the Massive MIMO Application Framework supports up to 20 MHz of instantaneous real-time bandwidth that scales from 8 to 128 antennas and can be used with multiple independent UEs. The LTE-like protocol employed uses a 2,048 point fast Fourier transform (FFT) and 0.5 ms slot time as shown in Table 1. The 0.5 ms slot time ensures adequate channel coherence and facilitates channel reciprocity in mobile testing scenarios (in other words, the UE is moving).

2.1. Massive MIMO Hardware and Software Elements

Designing a massive MIMO system requires four key attributes:

1. Flexible SDRs that can acquire and transmit RF signals
2. Accurate time and frequency synchronization among the radio heads
3. A high-throughput deterministic bus for moving and aggregating large amounts of data
4. High-performance processing for PHY and media access control (MAC) execution to meet the real-time performance requirements

Ideally, these key attributes can also be rapidly customized for a wide variety of research needs.

The NI-based Massive MIMO Application Framework combines SDRs, clock distribution modules, high-throughput PXI systems and LabVIEW to provide a robust, deterministic prototyping platform for research. This section details the various hardware and software elements used in both the NI-based massive MIMO base station and UE terminals.

USRP Software Defined Radio

The USRP RIO software defined radio provides an integrated 2x2 MIMO transceiver and a high-performance Xilinx Kintex-7 FPGA for accelerating baseband processing, all within a half width-1U rack-mountable enclosure. It connects to a host controller through cabled PCI Express x4 to the system controller

allowing up to 800 MB/s of streaming data transfer to the desktop or PXI Express host computer (or laptop at 200 MB/s over ExpressCard). Figure 2 provides a block diagram overview of the USRP RIO hardware.

USRP RIO is powered by the LabVIEW reconfigurable I/O (RIO) architecture, which combines open LabVIEW system design software with high-performance hardware to dramatically simplify development. The tight hardware and software integration alleviates system integration challenges, which are significant in a system of this scale, so researchers can focus on research. Although the NI application framework software is written entirely in the LabVIEW programming language, LabVIEW can incorporate IP from other design languages such as .m file script, ANSI C/C++, and HDL to help expedite development through code reuse.

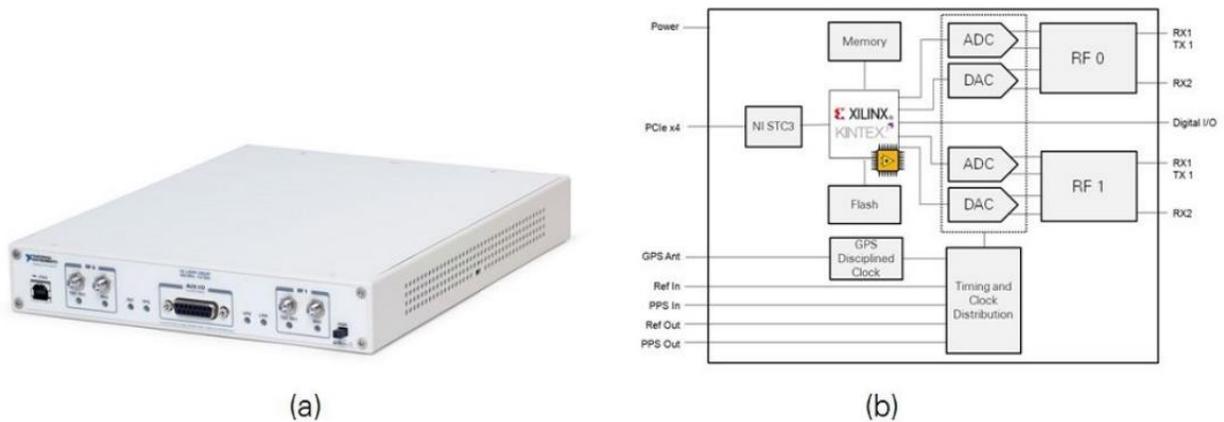


Figure 2-USRP RIO Hardware (a) and System Block Diagram (b)

PXI Express Chassis Backplane

The Massive MIMO Application Framework uses PXIe-1085, an advanced 18-slot PXI chassis that features PCI Express Generation 2 technologies in every slot for high-throughput, low-latency applications. The chassis is capable of 4 GB/s of per-slot bandwidth and 12 GB/s of system bandwidth. Figure 3 shows the dual-switch backplane architecture. Multiple PXI chassis can be daisy chained together or put in a star configuration when building higher channel-count systems.

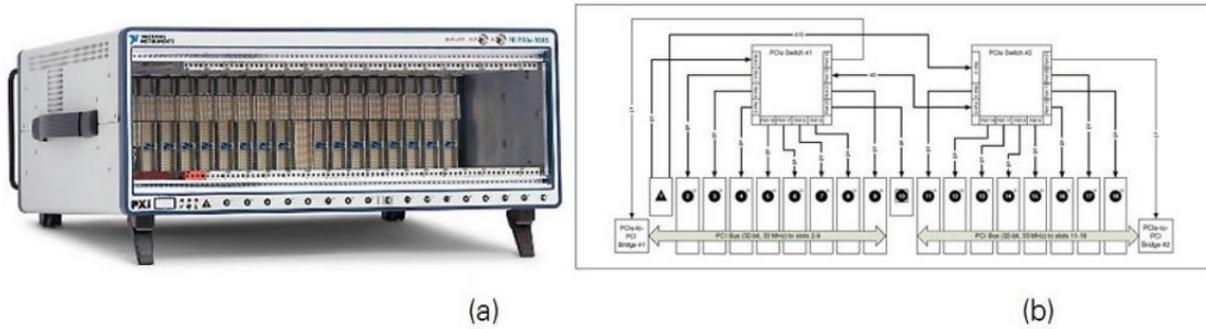


Figure 3-18-Slot PXIe-1085 Chassis (a) and System Diagram (b)

PCI Express Switch Box for USRP-RIO

CPS-8910 is a cabled PCI Express switch box for large MIMO expansion configurations and system control on the PXI and USRP platforms. Massive MIMO setups require the data to be aggregated in one location.. This module provides two PCI Express upstream ports and eight downstream ports for seamless system expansion. No programming is needed, and the switchbox can be used to aggregate up to 8 USRP-RIO into one stream. CPS-8910 is expected to mainly be used in large systems that incorporate dozens of USRPs in a massive MIMO configuration.



Figure 4 - Cabled PCI Express Switch Box between USRP-RIOs and PXI System

High-Performance Reconfigurable FPGA Processing Module

The Massive MIMO Application Framework uses FlexRIO FPGA modules to add flexible, high-performance processing modules, programmable with the LabVIEW FPGA Module, within the PXI form factor. The PXIe-7976R FlexRIO FPGA module can be used standalone, providing a large and customizable Xilinx Kintex-7 410T with PCI Express Generation 2 x8 connectivity to the PXI Express backplane. Many plug-in FlexRIO adapter modules can extend the platform's I/O capabilities with high-performance RF transceivers, baseband analog-to-digital converters (ADCs)/digital-to-analog converters (DACs), and high-speed digital I/O.

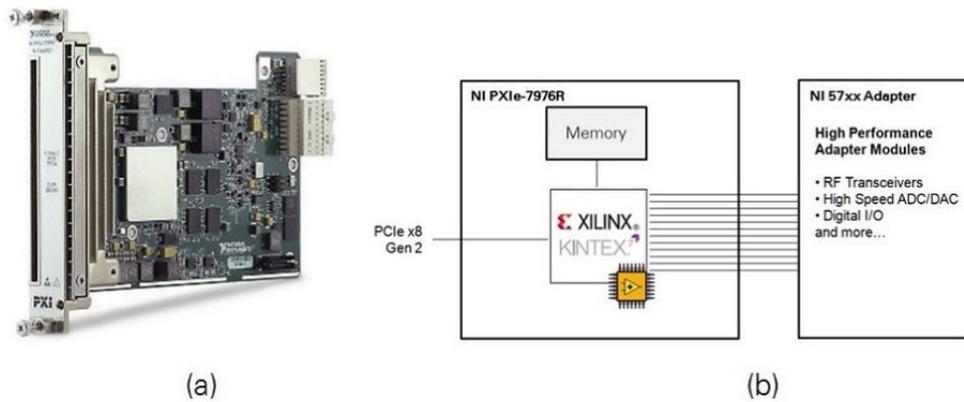


Figure 5-PXIe-7976R FlexRIO Module (a) and System Diagram (b)

Clock Synchronization Systems

The Massive MIMO Application Framework uses PXIe-6674T for generating high stability 10 MHz reference and precision pulse per second (PPS) master signals. These signals are distributed to USRP-RIOs through the Ettus Research OctoClock 8-channel clock distribution modules. OctoClocks provides both frequency and time synchronization for up to eight USRP devices by amplifying and splitting the master 10 MHz reference and pulse per second (PPS) signal eight ways through matched-length traces. The OctoClock-G adds an internal time and frequency reference using an integrated GPS-disciplined oscillator (GPSDO). Figure 5 shows a system overview of the OctoClock-G. A switch on the front panel gives the user the ability to choose between the internal GPSDO and an externally supplied reference. With OctoClock modules, users can easily build MIMO systems and work with higher channel-count systems that might include MIMO research among others.

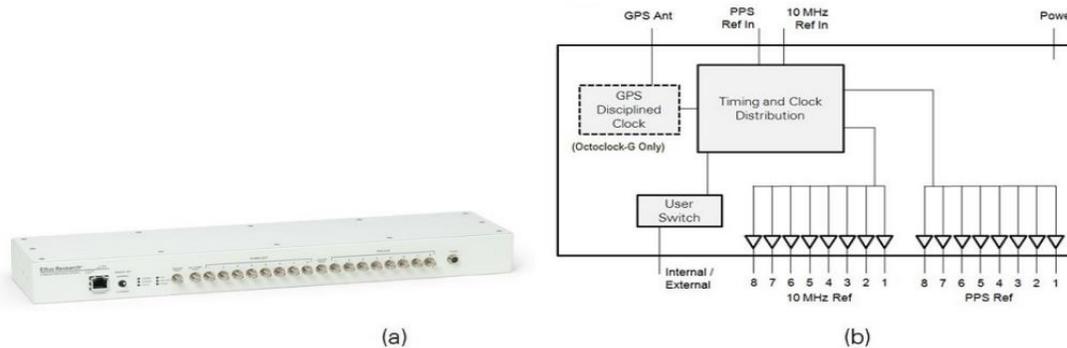


Figure 6-OctoClock-G Module (a) and System Diagram (b)

LabVIEW System Design Suite

LabVIEW provides an integrated tool flow for managing system-level hardware and software details; visualizing system information in a GUI, and developing general-purpose processor (GPP), real-time, and FPGA code; and deploying code to a research testbed. With LabVIEW, users can integrate additional programming approaches such as ANSI C/C++ through call library nodes, VHDL through the IP integration

node, and even .m file scripts through the LabVIEW MathScript RT Module. This makes it possible to develop high-performance implementations that are also highly readable and customizable. All hardware and software is managed in a single LabVIEW project, which gives the researcher the ability to deploy code to all processing elements and run testbed scenarios with a single environment. The Massive MIMO Application Framework uses LabVIEW for its high productivity and ability to program and control the details of the I/O via LabVIEW FPGA.

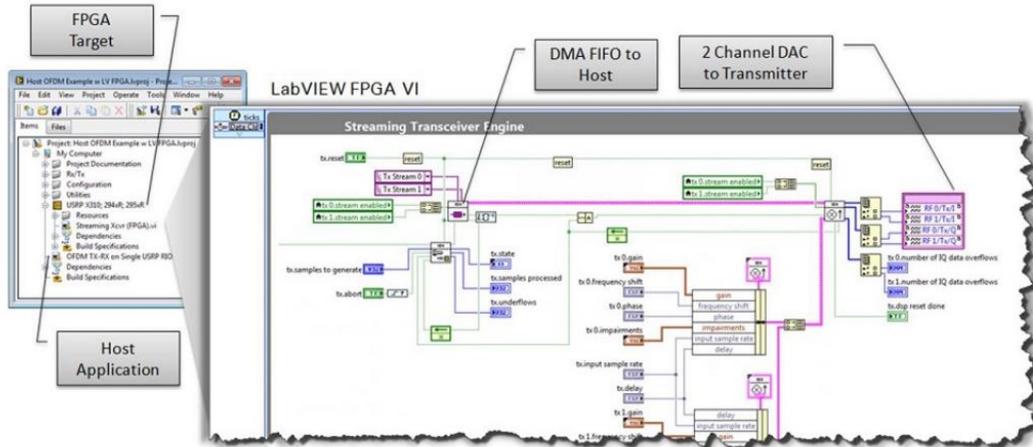


Figure 7-LabVIEW Project and LabVIEW FPGA Application

3. Massive MIMO BTS Application Framework Architecture

The hardware and software platform elements above combine to form an architecture that scales from a few antennas to more than 128 synchronized antennas. This document outlines 8-, 16-, 32-, 64- and 128-antenna configurations. Most dense 128-antenna system includes 64 dual-channel USRP RIO devices tethered to four PXI subsystem chassis configured in a star architecture. The master chassis aggregates data for centralized processing with both FPGA processors and a highest-performance PXI controller.

In Figure 7, the master uses the PXIe-1085 chassis as the main data aggregation node and real-time signal processing engine. The PXI chassis provides 17 slots open for input/output devices, timing and synchronization, FlexRIO FPGA boards for real-time signal processing, and PCIe extension modules to connect to the data aggregator switches. A 128-antenna massive MIMO BTS requires very high data throughput to aggregate and process I and Q samples for both transmit and receive on 128 channels in real time for which the PXIe-1085 is well suited, supporting PCI Generation 2 x8 data paths capable of up to 3.2 GB/s throughput.

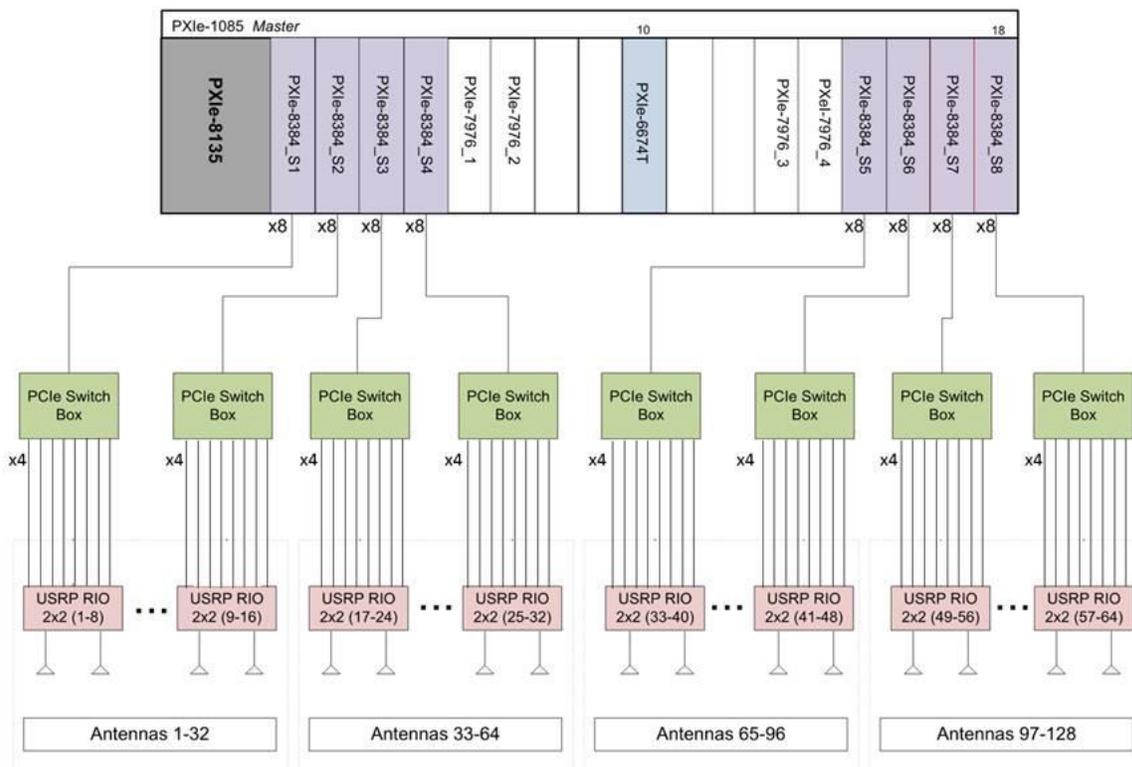


Figure 8-Scalable Massive MIMO System Diagram Combining PXI and USRP RIO

The master chassis houses four PXIe-8384 (S1 to S8) interface modules to connect to CPS-8910 PCI Express switch boxes to the master system. The connection between the chassis uses MXI and specifically PCI Express Generation 2 x8, providing up to 3.2 GB/s between the master and each PCIe switch box.

The system also features up to eight PXIe-7976R FlexRIO FPGA modules to address the real-time signal-processing requirements for the massive MIMO system. The slot locations provide an example configuration where the FPGAs can be cascaded to support data processing from each of the sub nodes. Each FlexRIO module can receive or transmit data across the backplane to each other and to all the USRP RIOs with < 5 microseconds of latency and up to 3 GB/s throughput.

For 8-, 16- channel lower antenna density configurations; a single Master PXIe chassis can accommodate all the required PXI modules for input/output devices, timing and synchronization, FlexRIO FPGA boards for real-time signal processing.

In Figure 8, the 16-channel MIMO system Diagram is provided as a reference for lower channel count system.

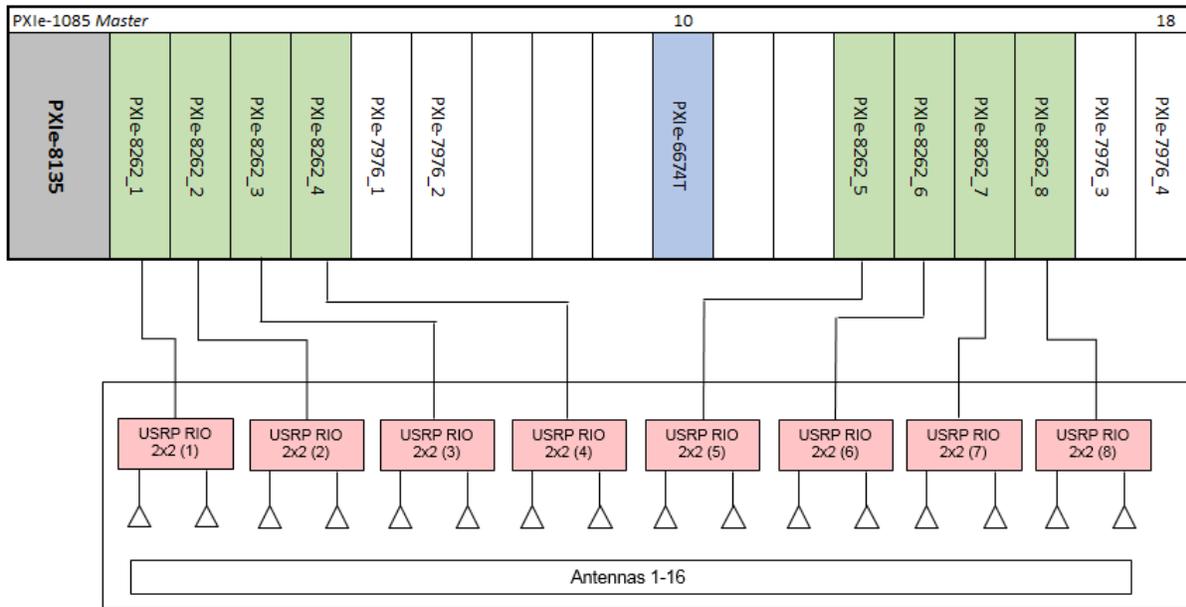


Figure 9 – A 16-Channel MIMO System Diagram

Although the sub-system components are removed; all the items within the lower channel count configurations can easily be upgraded to more dense systems by simply adding the subsystems and additional USRP-RIOs.

Timing and Synchronization

Timing and synchronization are important aspects of any system that deploys large numbers of radios; thus, they are critical in a massive MIMO system. The BTS system shares a common 10 MHz reference clock and a digital trigger to start acquisition or generation on each radio, ensuring system-level synchronization across the entire system (see Figure 9). The PXIe-6674T timing and synchronization module with OCXO, located in slot 10 of the master chassis, produces a very stable and accurate 10 MHz reference clock (80 ppb accuracy) and supplies a digital trigger for device synchronization to the master OctoClock-G clock distribution module. For channel configurations having more than 16 BTS antenna elements; the OctoClock-G supplies and buffers the 10 MHz reference (MCLK) and trigger (MTrig) to

OctoClock modules one through eight that feed the USRP RIO devices, thereby ensuring that each antenna shares the 10 MHz reference clock and master trigger. The control architecture proposed offers very precise control of each radio/antenna element.

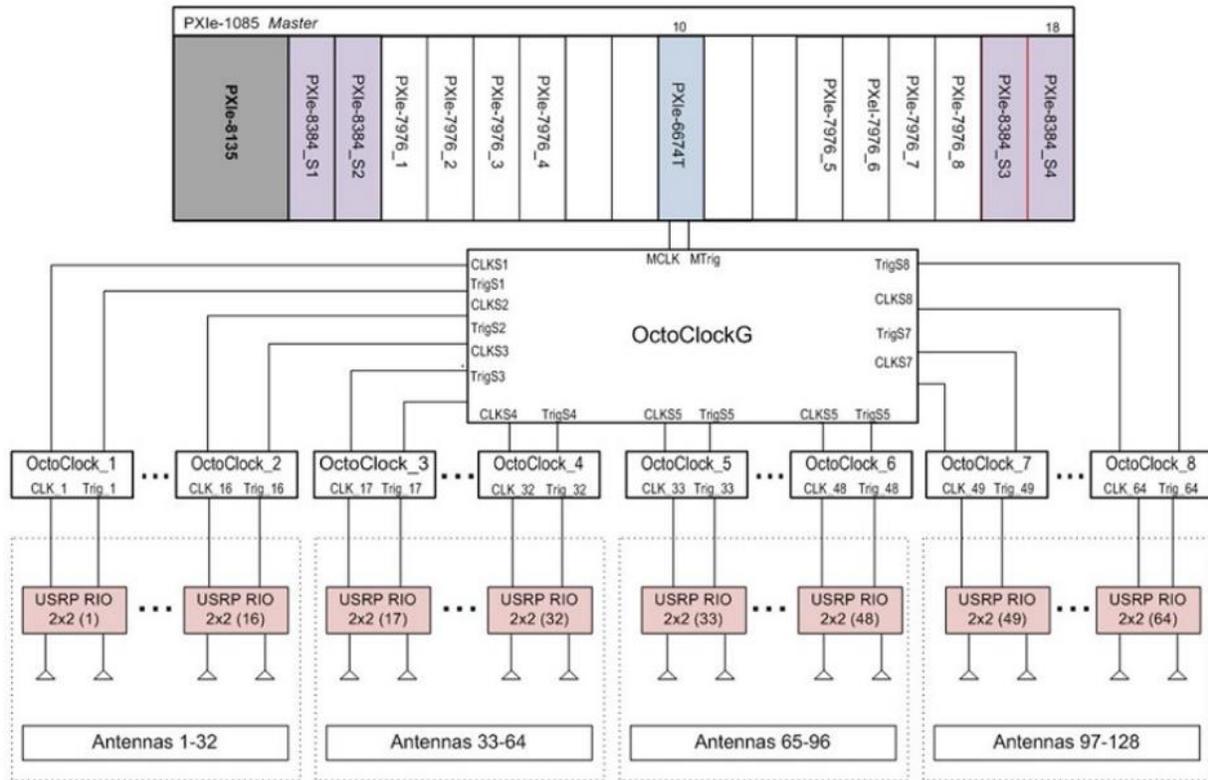


Figure 10 - Massive MIMO Clock Distribution Diagram (for 16+ antenna configurations)

For channel configurations up to 16 antenna arrays, a single OctoClock-G supplies and buffers the 10 MHz reference (MCLK) and trigger (MTrig) to one through eight of the USRP-RIO devices.

Table 2 provides a quick reference of the base station parts list for the 8-, 16-, 64-, 96-, and 128-antenna systems. It includes hardware devices and cables used to connect the devices as described in this section.

Description	Part No	Quantity for Each Antenna Configuration				
		8	16	32	64	128
PXIe-1085 <i>18 Slot 3U Chassis, 24 GB/s BW</i>	783588-01	1	1	1	1	1
Chassis Rack-Mount Assembly <i>Front or Back Mount Options</i>	778644-01 778644-02	1	1	1	1	1
PXI Power Cord <i>240V, 10A, Euro, Right Angle</i>	763067-01	1	1	1	1	1
PXIe-8135 <i>Core i7-3610QE Win7 Controller</i>	782450-04	1	1	1	1	1
8 GB RAM Upgrade for PXIe-8135	782341-8192	1	1	1	1	1
PXIe-7976R <i>LabVIEW FPGA Programmable Module (Xilinx Kintex-7 410T)</i>	783625-01	4	4	4	4	8
PXIe-6674T <i>Timing and Synchronization Module</i>	781037-01	1	1	1	1	1
USRP-2943R <i>2-Antenna LabVIEW FPGA Programmable SDR (1.2÷6GHz)</i>	783148-01	4	8	16	32	64
USRP-RIO Rack-Mount Assembly <i>Mounting Kit per Qty.2 USRP-RIO</i>	783492-01	2	4	8	16	32
2.4 and 5 GHz Dual Band Vertical Antenna	781913-01	8	16	32	64	Not Recom.
Power Cord for USRP-RIO	783490-01	4	8	16	32	64
PXIe-8262 <i>x4 MXI-Express Daisy-Chain Copper Interface with 3m. Cable</i>	780064-01	4	8	0	0	0
CPS-8910 <i>x4 PCI Express Switch Box</i>	784307-01	0	0	2	4	8
X4 MXI-Express Cable (3m) <i>for use between CPS-8910 and USRP-RIO</i>	779725-03	0	0	16	32	64
PXIe-8384 <i>x8 Gen2 MXI-Express for PXI Express Interface</i>	782363-01	0	0	2	4	8
x8 MXI-Express Cable (3m) <i>for use between CPS-8910 and PXIe-8384</i>	782317-03	0	0	2	4	8
Octoclock <i>8-Channel Clock Distribution System</i>	782978-01	0	0	4	4	8
Octoclock-G <i>8-Channel Clock Distribution System with GPSDO</i>	782979-01	1	1	1	1	1
SMA-SMA Cable (1m)	783469-01	26	34	50	82	146

Table 2 - Massive MIMO Base Station Options Parts List

4. BTS Software Architecture

The base station application framework software is designed to meet the system objectives outlined in Table 1 with OFDM PHY processing distributed among the FPGAs in the USRP RIO devices and MIMO PHY processing elements distributed among the FPGAs in the PXI master chassis. Higher level MAC functions run on the Intel-based general-purpose processor (GPP) in the PXI controller. The system architecture allows for large amounts of data processing with the low latency needed to maintain channel reciprocity. Precoding parameters are transferred directly from the receiver to the transmitter to maximize system performance.

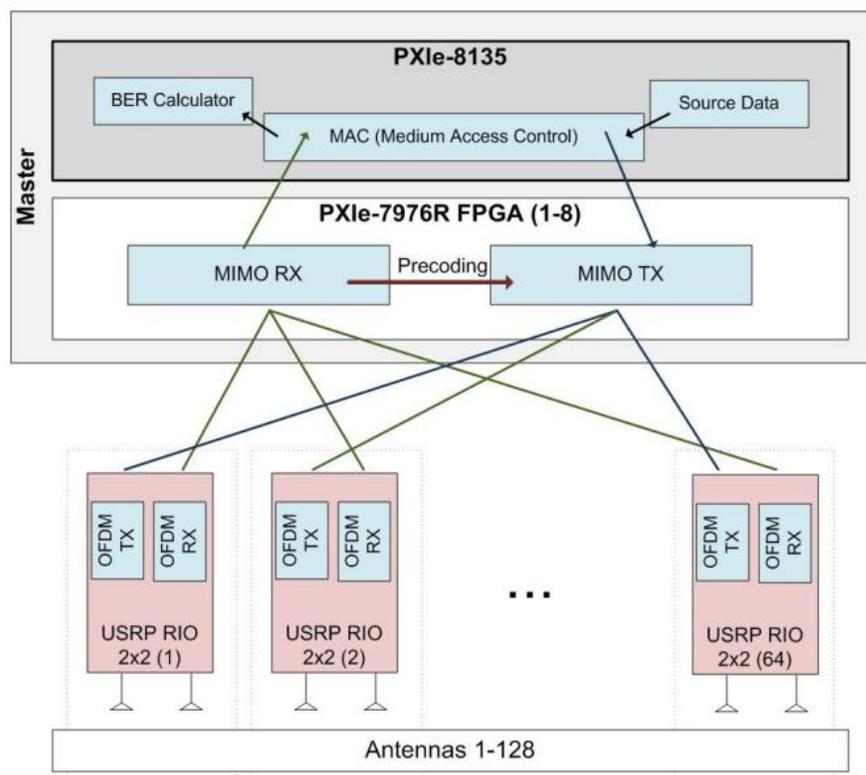


Figure 11 - Massive MIMO Data and Processing Diagram

Starting at the antenna, the OFDM PHY processing is performed in the FPGA, which allows the most computationally intensive processing to happen near the antenna. The resulting computations are then combined at the MIMO receiver IP where channel information is resolved for each user and each subcarrier. The calculated channel parameters are transferred to the MIMO TX block where precoding is applied, focusing energy on the return path at a single user. Although some aspects of the MAC are implemented in the FPGA, the majority of it and other upper layer processing are implemented on the GPP. The specific algorithms being used for each stage of the system is an active area of research. The entire system is reconfigurable, implemented in LabVIEW and LabVIEW FPGA—optimized for speed without sacrificing readability.

4.1 Sample Application

Screenshots from a sample application of streaming video transfer from multiple UEs is presented in Figure 11 and 12. Notice that the application is based on the reference framework described through the this document.

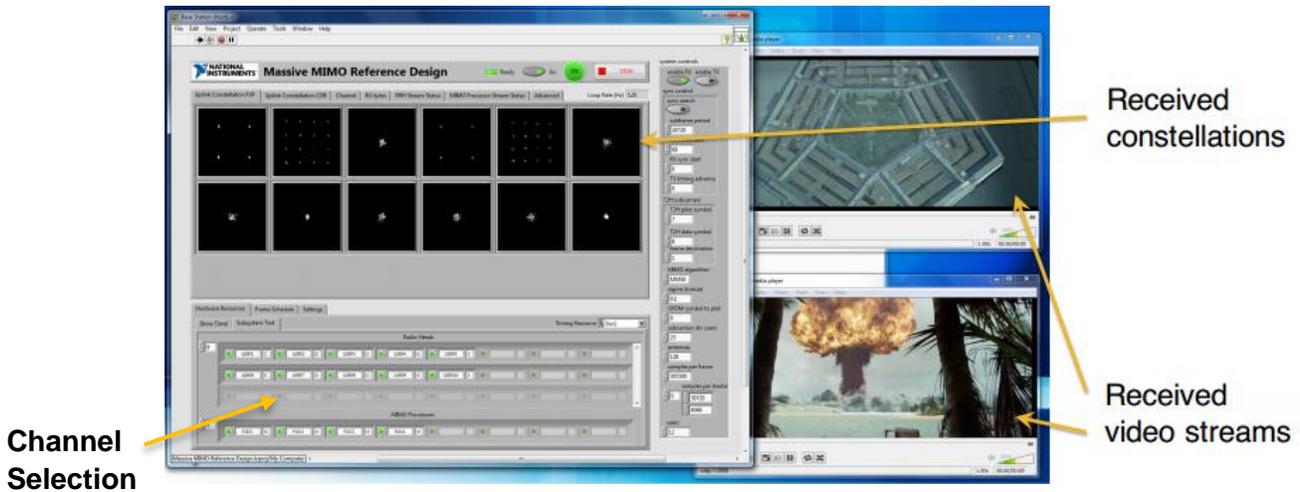


Figure 12 - Constellation of decoded user data (2 Video Streams received from UEs)

In this application; there are 12 plots to display constellations from up to 12 users. Users that are not present in the system appear as noisy dots centered at the origin. Also; as depicted in left; application can scale up to more BTS channels by simply adding the required hardware and enabling the channels. All sample routing, aggregation and disaggregation is taken care of under the hood.

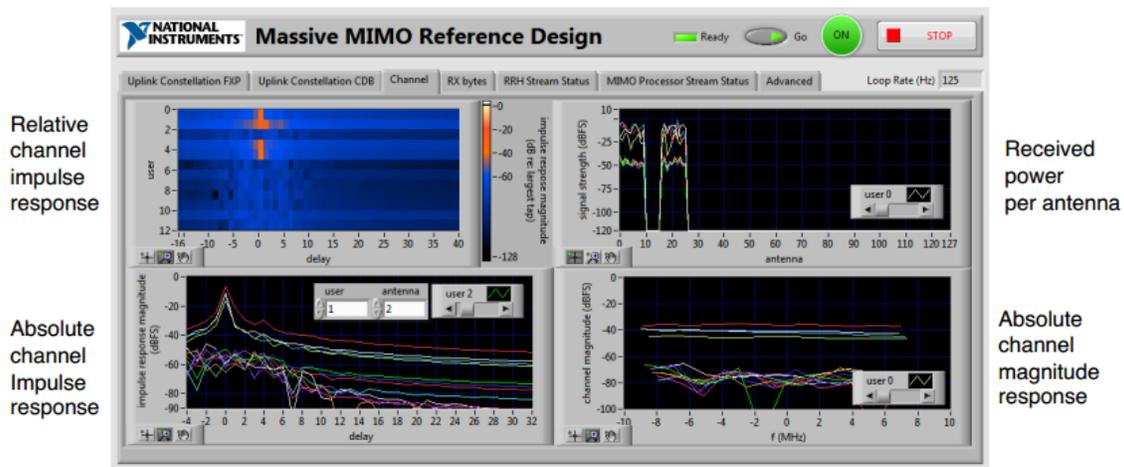


Figure 13 – Various Channel Measurements at Base Station

5. User Equipment (UE)

Each UE represents a handset or other wireless device with single input, single output (SISO) or 2x2 MIMO wireless capabilities. The UE prototype uses USRP RIO, with an integrated GPSDO, connected to a laptop using cabled PCI Express to an ExpressCard. The GPSDO is important because it provides improved frequency accuracy and enables synchronization and geo-location capability if needed in future system expansion. A typical testbed implementation would include multiple UE systems where each USRP RIO might represent one or two UE devices. Software on the UE is implemented much like the BTS; however, it is implemented as a single antenna system, placing the PHY in the FPGA of the USRP RIO and the MAC layer on the host PC.

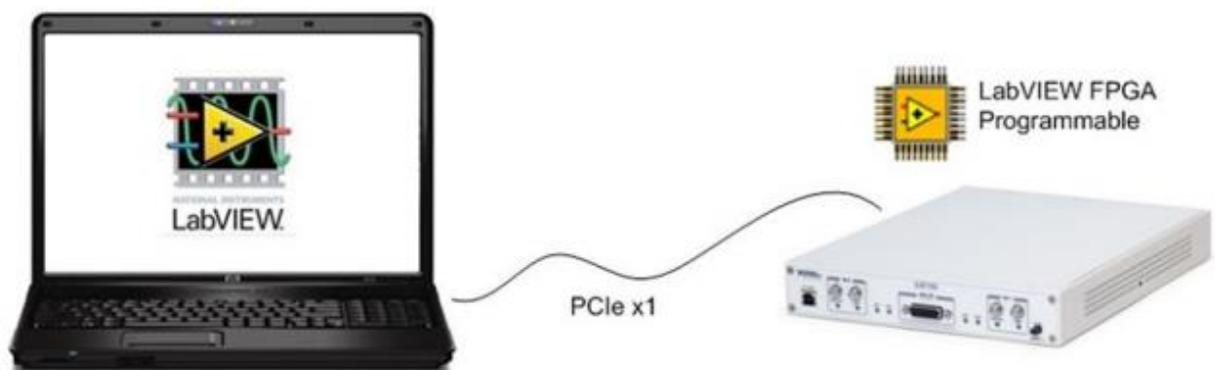


Figure 14 - Typical UE Setup With Laptop and USRP-RIO

Table 3 provides a quick reference of parts used in a single UE system. It includes hardware devices and cables used to connect the devices as shown in Figure 10. Alternatively, a PCI Express connection can be used if a desktop is chosen for the UE controller.

Description	Part No	Quantity for Each User Equipment
USRP-2943R 2-Antenna LabVIEW FPGA Programmable SDR (1.2÷6GHz)	783148-01	1
2.4 and 5 GHz Dual Band Vertical Antenna	781913-01	2
Power Cord for USRP-RIO	783490-01	1
USRP-RIO Laptop Connectivity Kit (ExpressCard and Cable)	783489-01	1
Laptop with ExpressCard Slot	User Supplied	1

Table 3 - UE Equipment List

6. Conclusion

NI technology is revolutionizing the prototyping of high-end research systems with LabVIEW system design software coupled with the USRP RIO and PXI platforms. This white paper demonstrates one viable option for building a massive MIMO system in an effort to further 5G research. The unique combination of NI technology used in the application framework enables the synchronization of time and frequency for a large number of radios and the PCI Express infrastructure addresses throughput requirements necessary to transfer and aggregate I and Q samples at a rate over 15.7 GB/s on the uplink and downlink. Design flows for the FPGA simplify high-performance processing on the PHY and MAC layers to meet real-time timing requirements.

To ensure that these products meet the specific needs of wireless researchers, NI is actively collaborating with leading researchers and thought leaders such as Lund University. These collaborations advance exciting fields of study and facilitate the sharing of approaches, IP, and best practices among those needing and using tools like the Massive MIMO Application Framework.

Read more solutions at [ni.com/5g](http://www.ni.com/5g) (<http://www.ni.com/5g>).

7. Contact Information

For further details, price inquiries and product demonstrations; feel free to contact NI through the following channels:

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